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PATENT

Attorney Docket No. Y0R920000402US1 (8728-497)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Peter W. Cook Group No.: 2115
Serial No.: 09/836,375 Examiner: Suryawanshi, Suresh
Filed: April 17, 2001 Date of mailing of "Notice of Allowance and
Base Issue Fee Due" September 1, 2004
Confirmation No. 5195
For LATCH STRUCTURE FOR INTERLOCKED PIPELINED
CMOS (IPCMOS) CIRCUITS

MAIL STOP ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF FORMAL DRAWINGS

Attached please find twelve (12) sheets of formal drawings for the above-identified application.

Please charge any deficiency as well as any other fee(s) which may become due under 37 C.F.R. § 1.16 and/or 1.17 at any time during the pendency of this application, or credit any overpayment of such fee(s) to Deposit Account No. 50-0510/IBM.
TWO (2) COPIES OF THIS SHEET ARE ENCLOSED.



SIGNATURE OF ATTORNEY

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(Transmittal of Formal Drawings [5-2])